SEMICONDUCTOR DEVICE USING A NITRIDE SEMICONDUCTOR

CROSS REFERENCE TO RELATED APPLICATION

This application claims benefit of priority under 35USC §119 to Japanese Patent Application No. 2004-54330, filed on Feb. 27, 2004, the contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, for example, to an insulating gate type field effect transistor using a nitride semiconductor.

2. Related Background Art

Since a nitride semiconductor device using gallium nitride (hereinafter referred to simply as GaN) has a large band gap as compared with a semiconductor device using silicon (Si), the semiconductor device has a high critical electric field, and from this characteristic, a small-sized device having a high breakdown voltage is easily realized. Accordingly, in a semiconductor for electric power control, a low on-resistance is achieved, and a device having a low loss can be realized. Above all, in a field effect transistor using an AlGaN/GaN heterostructure (hereinafter referred to simply as an HFET (a heterostructure field effect transistor), satisfactory characteristics can be expected with a simple device structure. A gate electrode in AN HFET has a Schottky gate structure forming a Schottky junction with an AlGaN layer. Moreover, a conventional GaN-based HFET is a normally on-type device in which a current flows between a source and a drain, when a drain voltage is applied at a gate voltage of zero.

However, in general, the Schottky gate structure has a problem that a leak current increases, when a gate leak current is large and device temperature rises. A normally-on type device has a problem that a large current flows at the moment at which a power to a circuit is turned on, and this sometimes results in destruction of the device.

BRIEF SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a semiconductor device comprising:

a first semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$);

a first conductivity type or non-doped second semiconductor layer represented by a composition formula $Al_yGa_{1-y}N$ ($0 \leqq y \leqq 1$, $x<y$) and is formed on the first semiconductor layer;

a second conductivity type third semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$($0 \leqq x \leqq 1$) and is selectively formed on the second semiconductor layer;

a gate electrode formed on the third semiconductor layer;

a source electrode electrically connected to the second semiconductor layer; and

a drain electrode electrically connected to the second semiconductor layer;

wherein the distance between the drain electrode and the third semiconductor layer is longer than the distance between the source electrode and the third semiconductor layer.

According to a second aspect of the present invention, there is provided a semiconductor device comprising:

a first semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$);

a first conductivity type or non-doped second semiconductor layer represented by a composition formula $Al_yGa_{1-y}N$ ($0 \leqq y \leqq 1$, $x<y$) and is formed on the first semiconductor layer;

a second conductivity type third semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) and is selectively formed above the second semiconductor layer;

a gate insulator formed on the third semiconductor layer;

a gate electrode formed on the gate insulator;

a source electrode electrically connected to the second semiconductor layer; and a drain electrode electrically connected to the second semiconductor layer.

According to a third aspect of the present invention, there is provided a semiconductor device comprising:

a first semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$);

a first conductivity type or non-doped second semiconductor layer represented by a composition formula $Al_yGa_{1-y}N$ ($0 \leqq y \leqq 1$, $x<y$), formed on the first semiconductor layer and having a concave portion;

a second conductivity type third semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) and is selectively formed above a bottom surface of the concave portion of the second semiconductor layer;

a gate electrode formed on the third semiconductor layer;

a source electrode electrically connected to the second semiconductor layer; and a drain electrode electrically connected to the second semiconductor layer.

According to a fourth aspect of the present invention, there is provided a semiconductor device comprising:

a first conductivity type or non-doped first semiconductor layer represented by a composition formula $Al_yGa_{1-y}N$ ($0 \leqq y \leqq 1$, $x<y$), the first semiconductor layer having a first surface and a second surface opposite to the first surface, and further having a concave portion on the side of the first surface;

a second conductivity type second semiconductor layer represented by a composition formula $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) and is formed on the second surface of the first semiconductor layer;

a gate electrode formed above a bottom surface of the concave portion of the first semiconductor layer;

a source electrode electrically connected to the first semiconductor layer; and a drain electrode electrically connected to the first semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a sectional view schematically showing a first embodiment of a semiconductor device according to the present invention;

FIG. **2** is a sectional view schematically showing a first modification of the semiconductor device shown in FIG. **1**;

FIG. **3** is a sectional view schematically showing a second modification of the semiconductor device shown in FIG. **1**;

FIG. **4** is a sectional view schematically showing a second embodiment of a semiconductor device according to the present invention;

FIG. **5** is a sectional view schematically showing a modification of the semiconductor device shown in FIG. **4**;